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Electron Multiplying Low Voltage CCD with Increased Gain

Konstantin D. Stefanov, *Member, IEEE*, Alice Dunford and Andrew D. Holland

Abstract—Novel designs for the gain elements in electron multiplying (EM) CCDs have been implemented in a device manufactured in a low voltage CMOS process. Derived with help from TCAD simulations, the designs employ modified gate geometries in order to significantly increase the EM gain over traditional structures. Two new EM elements have been demonstrated with an order of magnitude higher gain than the typical rectangular gate designs, achieved over 100 amplifying stages and without an increase in the electric field. The principles presented in this work can be used in CMOS and CCD imagers employing electron multiplication in order to boost the gain and reduce undesirable effects such as clock-induced charge generation and gain ageing.

Index Terms—Electron multiplying charge coupled devices (EMCCDs), impact ionization.

I. INTRODUCTION

ELECTRON Multiplying Charge Coupled Devices (EMCCDs) are widely used in photon-starved applications due to their ability to achieve deep sub-electron readout noise (<0.2 e⁻ RMS), allowing single photon detection at video frame rates [1]. In EMCCDs the photogenerated charge is amplified by impact ionization (II) as it passes through a modified serial readout register, with the gain being typically about 1% per EM stage. After hundreds of stages the signal can be amplified by a factor as large as several thousand, and this gain effectively reduces the readout noise of the output amplifier.

EMCCDs have been available commercially for nearly two decades and are staple in numerous applications requiring low light level imaging. Recently, devices with similar functionality have been implemented in CMOS technology, taking advantage of the smaller feature sizes of the manufacturing processes and introducing new ideas such as reciprocating charge transfer and EM within a pinned photodiode [2][3].

Fig. 1 shows the operating principles and the typical structure of the gain element in EMCCDs, built as a 4-phase device. Electrons stored under P1 are transferred through a region with high electric field developed between P2DC and P2HV, causing II in the process. Typically only a small

fraction of the transferred electrons, of the order of one percent on average, undergoes II. The gate P2DC is held static, while P2HV is clocked with voltages which could exceed 40 V in some EMCCDs. The gates P1 and P3 are operated with normal clock amplitudes. This clocking scheme is necessary because the region of high electric field has to be established before the charge passes through it. It takes only a few nanoseconds for the majority of the electrons to transfer from one gate to the next, and this is usually much shorter than the rise time of the gate voltages. If one gate in a CCD is simply driven to a high voltage without maintaining a potential barrier in front of it as shown in Fig. 1, most of the electrons will be transferred before the field becomes high enough, resulting in little or no EM gain.

The P2HV voltage is selected in order to achieve the desired EM gain, typically in the 100 to 1000 range, using several hundred amplifying stages. Commercial devices are routinely operated at pixel rates reaching 30 Mpix/s using suitable high voltage drivers, while keeping the power dissipation acceptable. Many practical aspects of EMCCD operation and their supporting circuits are given in [4]. The gain is controlled by the electrical field developed between P2DC and P2HV, and can be increased by higher potential difference or by reducing the inter-gate gap. However, maximizing the electric field is not the best route to higher gain because several undesirable effects begin to appear, as described below. Achieving a balance between the target EM gain while keeping the secondary effects in check is very important for good device performance.

Despite the recent advances in CMOS image sensors with ultrahigh conversion gain and sub-electron readout noise [5][6], EMCCDs are superior in many photon-counting applications, such as single cell or molecule imaging [7]. They are also considered for the WFIRST space telescope aiming to directly detect exoplanets [8]. The challenges in such demanding applications are to minimize the effects from two of the main shortcomings of EMCCDs – generation of spurious clock-induced charge (CIC) [8] and gain ageing [9].

CIC occurs due to parasitic II in the multiplication register, as well as in the image area where no high voltages are used. The source of CIC are holes which can be accelerated by high electric fields on their return from interface traps to the channel stops and undergo II, with the electrons collected as parasitic charge. The standard practice to prevent this in the multiplication register is by enclosing the HV gate completely within the CCD buried channel [10], as shown in Fig. 1(c).

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Konstantin D. Stefanov, Alice Dunford and Andrew D. Holland are with the Centre for Electronic Imaging (CEI), The Open University, Walton Hall, Milton Keynes, MK7 6AA, UK (e-mail: Konstantin.Stefanov@open.ac.uk).

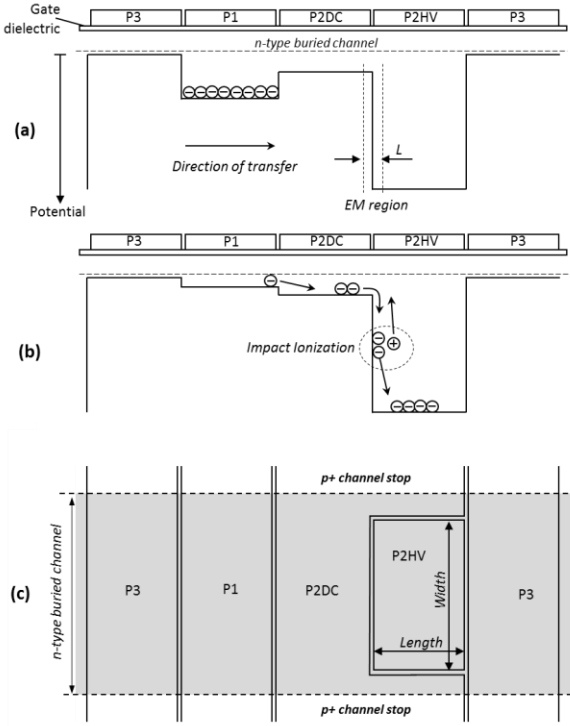


Fig. 1. Cross section and a potential diagram of an EMCCD gain element before (a) and during charge transfer (b), when II occurs. Top view of the gain element (c).

This is crucial for reducing the average CIC below 10^{-2} e-/pixel, suitable for a practical device, but the parasitic signal can still be detrimental in single photon imaging using high EM gains.

Ageing is an undesirable decrease of EM gain over time, attributed to injection of hot carriers into the gate dielectric and creation of defects at the Si-SiO₂ interface by them. Trapped holes under P2DC or trapped electrons under P2HV decrease the effective potential difference [11], leading to lower EM gain.

Both CIC and ageing are exacerbated at high EM gains because the impact ionization rate increases exponentially with the electric field [12]. Naturally, the voltage applied at the HV gate should be kept as low as possible to reduce any detrimental effects, however this reduces the EM gain as well. Instead, it could be possible to employ techniques aimed at increasing the EM gain while keeping the same high voltage, or conversely, to reduce the voltage at the same gain. This is expected to lead to reduced CIC, gain ageing and power dissipation, and is the subject of this paper.

II. DESIGN CONSIDERATIONS

A. Simulations of Charge Transport in EMCCDs

Simulations with TCAD tools can reveal a great deal of information about the EM process, showing the path electrons take through the structure, the electrostatic potential, and where EM occurs [11]. Further detail can be obtained from simulations in 3D and this is essential for the visualization of the electron path.

Figure 2 shows a simulation of an EMCCD gain element

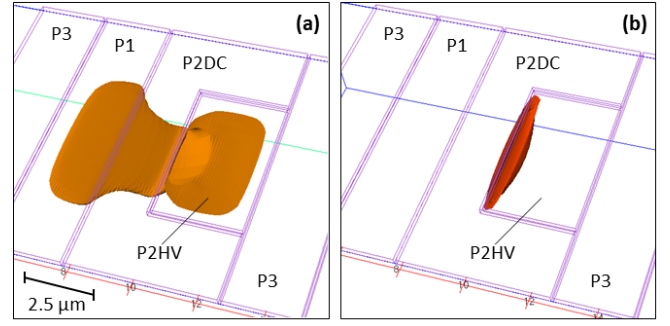


Fig. 2. TCAD simulation of an EM gain element using the design in Fig. 1(c) showing iso-surfaces of the electron concentration at 10^{12} cm^{-3} (a) and the impact ionization rate at $10^{21} \text{ cm}^{-3} \text{ s}^{-1}$ (b) at a moment in time when 50% of the charge has been transferred from P1 to P2HV. The signal charge is 900 e-.

midway through the transfer process as the charge moves from P1 to P2HV. The simulation was performed using tools from [13] for a model representative for the device described in Section III. Figure 2(a) shows an iso-surface of the electron concentration at 10^{12} cm^{-3} , where it can be seen that the path taken by the electrons is nearly as wide as the leading edge of P2HV. Figure 2(b) shows an iso-surface of the impact ionization rate at the same time, where it is apparent that most of the EM occurs at the leading edge of P2HV near the center of the gate.

Fig. 3 displays the electric field and the electron concentration in a cross section through the middle of the buried channel for the model in Fig. 2 at the same point in time. Significant EM only occurs at depths up to $0.4 \mu\text{m}$ below the Si-SiO₂ interface, as further down the electric field drops below 10^5 V/cm . The electric field responsible for EM is almost entirely determined by the size of the inter-electrode gap and the voltages applied to the gates.

We can see that most of the signal electrons skim past the region with the highest electric field developed near the inter-gate gap, and undergo II at fields much lower than the maximum available in the device. In the presented simulation the charge is completely transferred from P1 to P2HV in 2 ns, and spends even shorter time in the high field region. The path

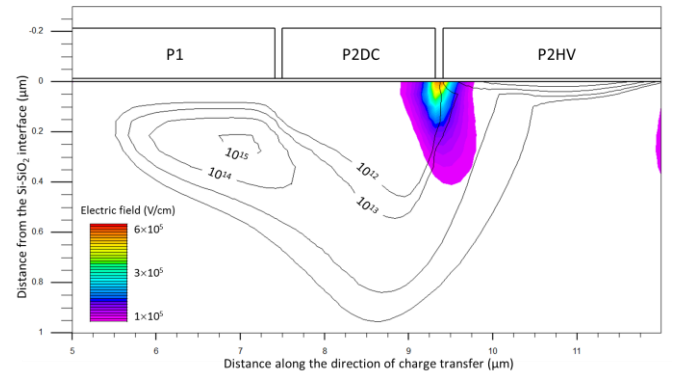


Fig. 3. Electric field and electron concentration (in cm^{-3} , presented as black contour lines) corresponding to Fig. 2, with P2HV = 15 V and P2DC = 2 V. The field developed in the gap between P2HV and P3 on the right (not fully shown) is similar to the field between P2HV and P2DC, but does not take part in the EM process.

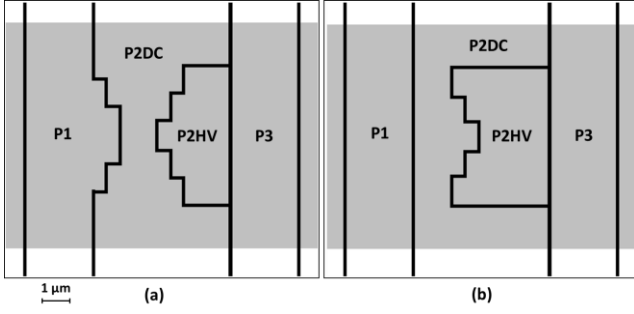


Fig. 4. Proposed gate geometries for increased EM gain: “spike” (a) and “staircase” (b). The inter-gate gap is drawn as a thick black line, and the buried channel is indicated by the grey shaded area.

of the electrons is inevitably towards P2HV where the potential is the highest, and where they get stored around the center of the gate. This trajectory does not fully overlap the region with the highest electric field, and is not optimal for achieving the highest EM gain.

The observations in Fig. 2 and Fig. 3 present at least two possible avenues to address the desired increase of EM gain.

One possibility follows from considering the expression (1) [12] for the electron-hole generation rate G from impact ionization, showing that it is proportional to the electron current density J_n . In (1) α_n is the ionization rate for electrons and q is the elementary charge. Impact ionization by holes is ignored because it is at least an order of magnitude lower than that of electrons at low electric fields [14][15].

$$G = \alpha_n J_n / q \quad (1)$$

In principle, if J_n could be increased while keeping everything else the same, G should increase too. This can be achieved by changing the shape of the P2DC and P2HV electrodes so that the signal electrons are coerced to travel in a narrower path when crossing under the P2DC-P2HV gap. An example of such design is shown in Fig. 4(a), and the corresponding simulation result is in Fig. 5(a) and Fig. 5(b). The “spike” protrusions from P1 and P2HV towards P2DC change the potential distribution so that small signal packets are transported in a narrow path around the center of the buried channel. This is effective in increasing the current density, and we can see in Fig. 5(b) that the region with the highest impact ionization rate largely coincides with the electron path. This is the desired distribution as it increases the probability that an electron can cause impact ionization.

The second possibility is to try to increase the chance of EM by increasing the effective length of the high field region L in Fig. 1(a), but without changing the magnitude of the field itself. As shown in [16] from basic considerations, the EM gain is exponentially dependent on L , therefore even a modest increase could substantially boost the gain.

In Fig. 2(a) we can see that the charge flow crosses perpendicularly to the inter-gate gap, spending minimum time under it. However, if the leading edge of P2HV is not straight, so that in certain parts the electrons could travel at a smaller angle to the gap or even parallel to it, the time spent in or near a high-field region could increase, thus increasing the effective length L . The design in Fig. 4(b) achieves that by breaking the leading edge of P2HV into 9 segments, 4 of which are parallel

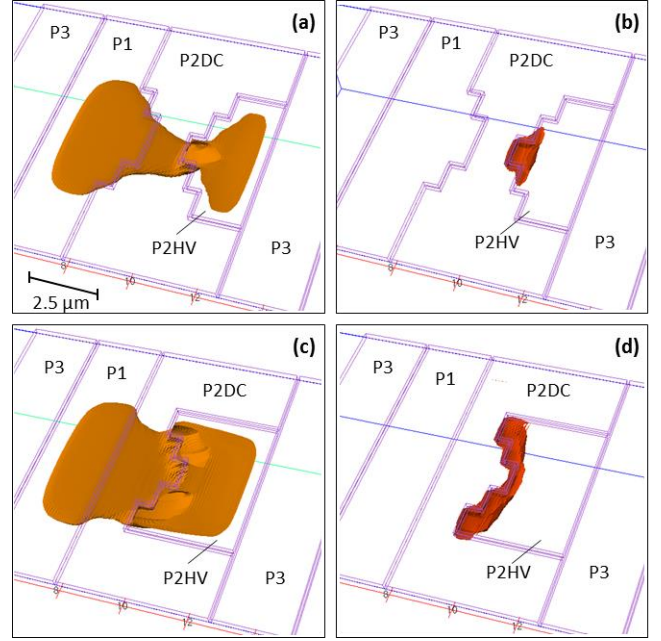


Fig. 5. Simulation results for the designs in Fig. 4: iso-surfaces of the electron concentration at 10^{12} cm^{-3} (a)(c); and impact ionization rate at $10^{21} \text{ cm}^{-3} \text{ s}^{-1}$ (b)(d) at a moment in time when 50% of the charge has been transferred from P1 to P2HV. The signal charge is 900 e-.

to the electron path. Fig. 5(c) and Fig. 5(d) show how the electron path and the ionization rate have been affected by this gate shape. In addition, the width of the electron flow is now wider compared to the simulation in Fig. 2(a) due to the increased gate area in the two leading corners, which changes the potential distribution. In Fig. 5(d) we can see that significant II occurs in both corners of the P2HV gate, in contrast with the rectangular design in Fig. 2(b). This change in the spatial distribution of the ionization rate is achieved without increasing the magnitude of the electric field, which is determined almost entirely by the potential applied across the fixed inter-gate gap.

It should be noted that both designs in Fig. 4 have identical number of segments in the leading edge of P2HV, four of which are parallel to the electron flow. Although the leading edge of P2HV in Fig. 4(a) is segmented too, the simulation in Fig. 5(a) indicates that only two of the four parallel edges could take any part in the EM process, while all four parallel edges are active in the design in Fig. 4(b). The markedly different electron flows suggests that any differences in EM gain are unlikely to be due only to the number of parallel edges used. Simulations indicate that the charge transfer times in the modified EM elements in Fig. 5 are nearly identical to the design in Fig. 2, given the same operating voltages.

By calculating the difference in the size of the signal packet after a transfer, with and without an impact ionization model turned on, the simulations presented in Fig. 5 indicate that the gain of the two new proposed EM elements is higher than in the traditional design in Fig. 2. However, quantifying the magnitude of the gain improvement was found to be unreliable due to the challenges in simulating II in sub-micrometer devices [17], further exacerbated by the conditions in EMCCDs, where the charge spends very short time in

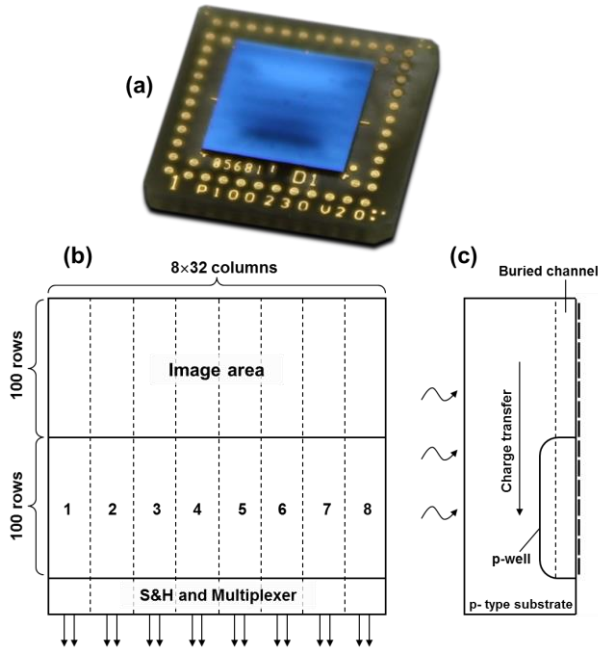


Fig. 6. Photomicrograph of the test chip bump-bonded to a carrier (a); simplified block diagram (b); cross section along the direction of transfer (c). Each EM element variant is indicated with its number and occupies a block of 32 columns. The size of the chip is 3.7 mm square.

relatively low electric fields.

Based on previous experience with commercial EMCCDs, achieving quantitative agreement between EM gains derived from simulations and data is very difficult. For these reasons, experimental verification of the described concepts was preferred.

B. Test Device

A chip containing column-parallel EMCCD on 10 μm pitch was designed by us and manufactured by ESPROS Photonics Corporation (EPC) [18], using 150 nm image sensor CMOS process. This technology features n-type buried channel CCDs in p-type high resistivity substrate with single level polysilicon CCD gates and 90 nm inter-electrode gaps. The CCD channel potential is only around 1.5 V, and this allows low voltage operation with gate clock amplitudes in the range between 2 V to 5 V. The choice of technology was driven by the small inter-gate gaps, allowing large electric fields to be obtained at low operating voltages.

The chip architecture, shown in Fig. 6, has been designed to provide a direct comparison between different EM elements operated simultaneously, and also includes reference elements without EM gain. The image area and pixel variants 1 and 2 are designed as a normal 4-phase CCD without EM elements, using gates on 2.5 μm pitch. Pixel variants 3 to 6 implement rectangular EM elements as in Fig. 1(c) with different P2HV sizes. Table I lists the dimensions of the P2HV gate for all the designs present on the chip. The width of the P2HV gate in

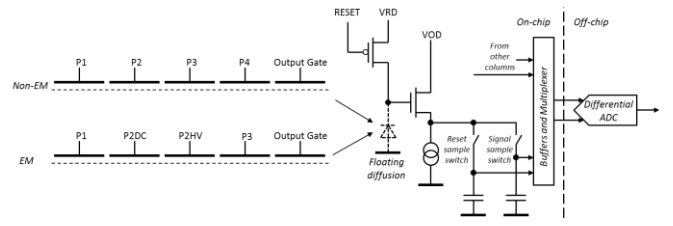


Fig. 7. Simplified readout circuitry of the test chip, showing the gate connections to the non-EM and EM columns. Correlated double sampling is performed by the differential ADC which subtracts the reset sample from the signal sample.

designs 5 to 8 is the same, allowing close comparison.

TABLE I
DIMENSIONS OF THE STUDIED EM ELEMENTS. DESIGNS 1 AND 2 ARE NORMAL 4-PHASE CCD ELEMENTS WITHOUT EM GAIN

Design	P2HV Length (μm)	P2HV Width (μm)	Drawing
1 and 2	-	-	No EM
3	3	6	Fig. 1(c)
4	2.5	6	Fig. 1(c)
5	3	5	Fig. 1(c)
6	2.5	5	Fig. 1(c)
7	“Staircase”	5	Fig. 4(b)
8	“Spike”	5	Fig. 4(a)

The chip is backside illuminated, with the bottom 100 rows placed in a p-well providing shielding from direct charge collection. In this way charge can enter the EM structures only from the image area above. Each column has its own sample and hold circuit to store the reset and the signal levels for off-chip correlated double sampling, as shown in Fig. 7. The stored signals from each block of 32 columns are multiplexed into a differential output for external digitization, using a 16-bit ADC operating at 500 kSa/s.

III. EXPERIMENTAL RESULTS AND DISCUSSION

The devices were found to function according to expectations and were characterized in the temperature range between -30 $^{\circ}\text{C}$ and +20 $^{\circ}\text{C}$. The EM gain was measured by using light-generated signal of approximately 900 electrons. After the charge had been collected in the image area, the device was read out at 10 kHz line rate. The gain was calculated from the difference between the output signals at the target P2HV amplitude and a much lower amplitude where EM does not occur, such as 4 V. The output signal is limited by the full well capacity of the device to approximately 90 ke-, and this constrains the achievable EM gain at a given input signal, and therefore also the amplitude of P2HV. No breakdowns were observed in any of the EM gate elements up to the maximum applied P2HV voltage of 15 V.

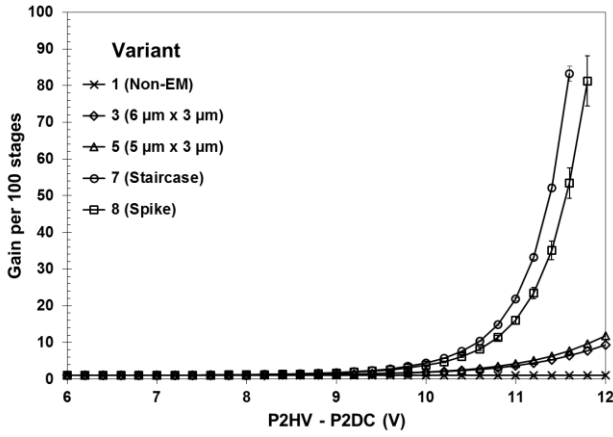


Fig. 8. EM gains measured with 900 e⁻ input signal at 0 °C as a function of the potential difference between P2HV and P2DC. The gain of each variant is averaged over 30 columns around the center of a block, and the error bars indicate the gain spread across the columns. All gates except P2HV were driven between 0.0 V and 4.0 V, and P2DC was fixed at 2.0 V.

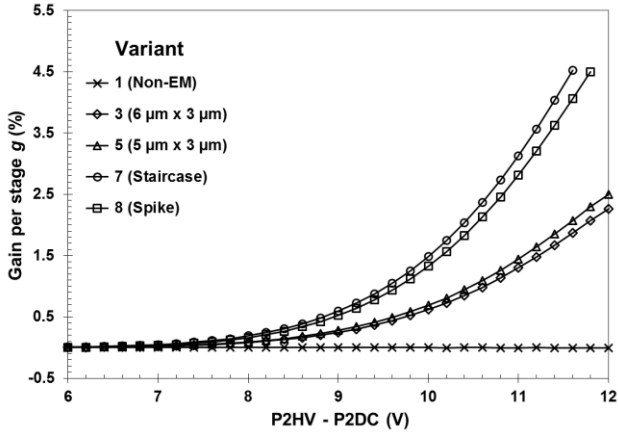


Fig. 9. EM gains per stage for the data in Fig. 8.

Fig. 8 shows the measured total gain after 100 stages for element types 3, 5, 7 and 8 (described in Table I) and the reference type 1, which does not have EM gain. Elements 3 to 6 have very similar performance and element 5 is used as the main EM benchmark because it has the same width and the most closely matching length to the two new elements 7 and 8.

The gain per stage g , plotted in Fig. 9, is the usual figure of merit as it provides data about the properties of the EM elements independently from the number of amplifying stages. The gain per stage is calculated from (2), where M is the total gain after n stages.

$$M = (1 + g)^n \quad (2)$$

The data show that the new EM elements 7 and 8 exhibit substantially increased gain compared to the two rectangular gate variants 3 and 5 under identical conditions. After 100 stages the total gain of EM element 7 is 10.7 times higher than that of EM element 5 at P2HV - P2DC = 11.6 V. This is a very significant difference given the small number of transfers. Furthermore, the gain advantage would theoretically grow to be several orders of magnitude higher after larger number of transfers (typically >500) used in commercial EMCCDs.

EM element 7 “staircase” outperforms element 8 “spike”,

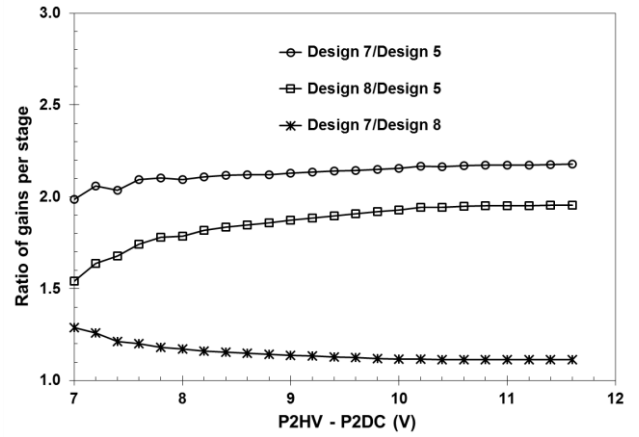


Fig. 10. EM gain ratio per stage for variants 7 and 8 relative to variant 5, and the ratio between variants 7 and 8 for the data in Fig. 8.

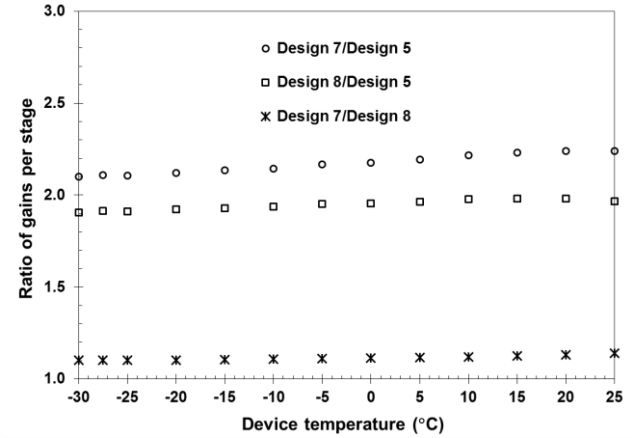


Fig. 11. EM gain ratio per stage for variants 7 and 8 relative to variant 5, and the ratio between variants 7 and 8 over the temperature range of the tests. The data were taken at P2HV - P2DC = 11 V and P2DC = 2 V.

which could not be resolved with confidence in the TCAD simulations due to difficulties with quantitative predictions, as mentioned in Section II.A. The experimental results suggest that increasing the effective length of the high field region, as implemented in the 4 edges in the “staircase” design, is more effective in increasing the EM gain than the combination of higher electron density with 2 parallel edges, as in the “spike” design. Figures 5(b) and 5(d) offer qualitative support for this conclusion.

We can also see that design 5 exhibits higher gain than design 3, with the only difference between them being the width of the P2HV gate. The narrower gate in design 5 forces the electron path into a smaller volume similarly to the “spike” design in Fig. 5(a) but not to the same extent, and this provides a reasonable explanation for the increased gain.

Figure 10 compares the relative performance of the different EM gain elements by plotting the gain ratios per stage as a function of the potential difference between P2HV and P2DC. The gain per stage can be written as (3) from (2), taking into account that $g \ll 1$, and is a convenient performance metric due to its proportionality to the logarithm of the total gain.

$$\frac{\ln(M)}{n} = \ln(1 + g) \approx g \quad (3)$$

The gain ratios shown in Fig. 10 remain almost constant over the voltage range where the EM gain is significant, as expected. Additional measurements of the gain ratios over the whole of the accessible temperature range, shown in Fig. 11, and with input signals up to 5 ke- did not reveal any anomalous behavior in any of the EM elements. The presented results are consistent over more than 10 chips tested in the course of the characterization. The spread of EM gain per stage over the tested devices was about 10%.

The gate shapes shown in Fig. 4 are presented in this paper due to the experimental verification of their performance, but are by no means the only possible designs. Other gate shapes can be considered, provided that they implement at least one of the underlying principles – constraining the electron flow to a smaller volume or increasing the effective length of the high field region.

It is important to note that the new designs achieve higher EM gain without increasing the magnitude of the electric field. The only changes involve the shapes of the P1 (for design 8), P2HV and P2DC gates over the buried channel, which does not alter the inter-gate gaps or the doping profiles in the device. The electric fields outside the buried channel should also remain the same, therefore we do not expect any inadvertent adverse effects. The CIC should be reduced correspondingly when lower P2HV amplitude is used to achieve the same EM gain, although this is hard to verify in our devices due to background from dark current even at the lowest achieved temperature.

TCAD simulations indicate that similar increase in gain from the two new EM elements is expected when applied to a typical EMCCD, which has much larger channel potential (usually >10 V) and operates with correspondingly higher voltages at the P2HV gate.

IV. CONCLUSION

New means of achieving higher EM gain in EMCCDs without increasing the magnitude of the electric field are studied by simulation and prototyped in a device built in a low voltage CMOS process. The increase in EM gain is caused by the developed novel gate shapes, which help increase the electron current density during transfer or the effective length of the high field region. Two new EM elements employing modified gate geometries have demonstrated significantly higher EM gains than the traditional rectangular gate EM elements under the same conditions. The presented designs and their derivatives can be used in both EMCCDs and CMOS image sensors using EM to help increase the gain, reduce the operating voltage, or both. This in turn is expected to lead to further performance improvements such as lower CIC, gain ageing and power dissipation.

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comments.

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